Remarks

In the final Office Action, the Examiner rejects claims 1-9 under 35 U.S.C. § 103(a) based on U.S. Patent No. 6,269,077 to Matsumura et al. ("Matsumura") in view of U.S. Patent No. 6,400,718 to Yamada et al. ("Yamada") and rejects claims 15-18 under 35 U.S.C. § 103(a) based on Yamada in view of Matsumura.

Claims 1-9 and 15-18 are currently pending.

As an initial point, Applicant submits that a rejection based on Matsumura is not a proper rejection under 35 U.S.C. § 103(a), as Matsumura does not qualify as prior art under 35 U.S.C. § 103(a). 35 U.S.C. § 103(c) qualifies 35 U.S.C. § 103(a) and states:

> (c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

(35 U.S.C. § 103(c)). Matsumura qualifies as prior art under 35 U.S.C. § 102 only under subsection (e), and Matsumura and the pending application were both initially assigned to NEC Corporation. Accordingly, Matsumura is not available to preclude patentability under 35 U.S.C. § 103(a).

Accordingly, the rejection of claims 1-9 based on Matsumura and Yamada under 35 U.S.C. § 103(a) and the rejection of claims 15-18 based on Yamada and Matsumura under 35 U.S.C. § 103(a).

Even assuming for the sake of argument that Matsumura was prior art under 35 U.S.C. § 103(a), Applicant submits, for the following reasons, that the

rejections of claims 1-9 and 15-18 under 35 U.S.C. § 103(a) are still improper and should be withdrawn.

Independent claim 1 is directed to a redundant system having two switch routes. The system includes N, with N greater than or equal to one, input selectors, each for receiving an input line and for connecting the received input line to one of the two switch routes based on a system switching signal. The system further includes a switch section for each one of the two switch routes, each of the switch sections having N input ports and N output ports, and N buffers. The N buffers each further include M, with M greater than or equal to two, priority queues for storing packets having different priorities. The system further includes an output selector for selecting one of the M priority queues from one buffer of one of the two switch sections. The system also includes a controller that receives status signals from both of the switch sections that includes information relating to a packet storing status of the M priority queues and, based on the status signals, controls the output selector to select the one of the M priority queues. The controller additionally generates the system switching signal.

Neither Matsumura nor Yamada, either alone or in combination, disclose or suggest each of the features recited in claim 1. For example, neither of these references discloses or suggests a switch section for each one of the two switch routes, as this switch section is recited in claim 1. More specifically, neither Matsumura nor Yamada discloses or suggests, as is recited in claim 1, a switch section having N input ports and N output ports, and N buffers that each further

include M, with M greater than or equal to two, priority queues for storing packets having different priorities.

Matsumura is directed to a switching system with a duplicated switch. (Matsumura, Abstract). Matsumura discloses a system including switching control units 21 and 31 for controlling which switching system is the standby system and which is the active system. (Matsumura, Fig. 1 and column 5, lines 47-52). In each of the duplicated switch sections, Matsumura also discloses temporary cell storage units 20 and 30. (Matsumura, Figs. 1 and 2). According to Matsumura, storage units 20 or 30 "temporarily stores incoming cells in each storage area depending on a delay class provided with each cell, and reads out each cell for switching from storage area in the order of higher delay priority to maintain the delay priority qualities of individual cells." (Matsumura, col. 4, lines 51-56). As shown in Fig. 2, temporary storage units 20 or 30 of Matsumura appear to each include a number of queues corresponding to different delay priorities.

Temporary storage units 20 or 30 of Matsumura, however, cannot be said to disclose or suggest a switch section having N input ports and N output ports, and N buffers that each further include M, with M greater than or equal to two, priority queues for storing packets having different priorities. Although temporary storage units 20 or 30 each appear to include a number of queues of buffers, labeled "DELAY PRIORITY M" through "DELAY PRIORITY N" in Fig. 2, the queues or buffers of Matsumura cannot be said to then further include "M priority queues," as recited in claim 1.

In rejecting claim 1, the Examiner contends that the switch section recited in claim 1 corresponds to temporary cell storage unit 20 of Matsumura and that the N buffers recited in claim 1 are shown in Figs. 1 and 2 of Matsumura as well as in lines 8-11 of claim 2 of Matsumura. (Office Action, page 3). Further, the Examiner contends that the M priority queues are disclosed by Matsumura in claim 2, lines 8-15, and in Figs. 2 and 3. (Office Action, page 3).

Fig. 2 of Matsumura, as discussed above, discloses temporary storage units 20 or 30 that each appear to include a number of queues or buffers, labeled "DELAY PRIORITY M" through "DELAY PRIORITY N." Fig. 3 is said by Matsumura to disclose "a block diagram illustrating the constitution of one example of the temporary cell storage unit 20 or 30 of the present invention. This temporary cell storage unit comprises … a temporary cell storage memory 202 to temporarily store input cells according to their delay classes." (Matsumura, col. 6, lines 30-32, 35, and 36). Applicant submits that temporary cell storage memory 202 of Matsumura appears to merely be an alternate illustration of temporary cell storage unit 20. Accordingly, queues or buffers within temporary cell storage memory 202 (Fig. 3 of Matsumura) cannot logically be said to correspond to the M priority queues recited in claim 1.

The N buffers recited in claim 1 and the M priority queues of claim 1 were cited by the Examiner as being disclosed by claim 2, lines 8-15 of Matsumura. Applicant disagrees. This portion of claim 2 of Matsumura discloses:

> temporary cell storage unit in each of active and stand-by systems for storing incoming cells in accordance with a delay priority provided with each cell transferred from said input selector; and
>
> system-switching control means for detecting cell information including delay priority stored in each temporary cell storage unit in

> both of active and stand-by systems, for instructing one of temporary cell storage units storing a cell having the highest delay priority among both of active and stand-by systems to read out the cell, and for outputting the read out cell from one of temporary cell storage units selectively to said output selector.

(Matsumura, claim 2, lines 8-19). This section of Matsumura recites the temporary cell storage unit. As previously discussed, the temporary cell storage unit is shown in Figs. 2 and 3 of Matsumura. This temporary cell storage unit does not disclose or suggest, as recited in claim 1, a switch section having N input ports and N output ports, and N buffers that each further include M, with M greater than or equal to two, priority queues for storing packets having different priorities.

For at least these reasons, Applicant submits that, contrary to the Examiner's contentions, Matsumura does not disclose or suggest, as recited in claim 1, a switch section having N input ports and N output ports, and N buffers that each further include M, with M greater than or equal to two, priority queues for storing packets having different priorities. Applicant submits that Yamada also does not disclose or suggest these features of claim 1. Accordingly, Matsumura and Yamada, even if combined as the Examiner suggests, do not disclose or suggest each of the features recited in claim 1. The rejection of claim 1 is therefore improper and should be withdrawn.

The rejections of claims 2-4 based on Matsumura and Yamada should also be withdrawn, at least by virtue of the dependency of these claims from claim 1.

Independent claim 5 and its dependent claims 6-9 were also rejected by the Examiner. Applicant respectfully traverses this rejection.

Claim 5 is directed to a packet switching system having two switch routes. The system includes N, with N greater than or equal to one, input selectors, each of which selects one of the two switch routes to connect N input lines to the selected switch route based on a system switching signal. The system further includes a switch section provided for each of the two switch routes, each of the switch sections having N input ports and N output ports and comprising N buffers, each of the N buffers further including a high-priority queue for storing input data units having a high-priority and a low-priority queue for storing input data units having a low priority. The system further includes a high-priority output selector coupled to the high priority queues in each of the switch sections; a low-priority output selector coupled to the low priority queues in each of the switch sections; a high-priority output queue for storing an output of the high-priority output selector; and a low-priority output queue for storing an output of the low-priority output selector. The system further includes a controller configured to generate the system switching signal and receive status signals from each of the two switch sections that include information relating to a storage status of the high-priority queues and the low-priority queues, the controller controlling the high-priority output selectors and the low-priority output selectors depending on the status signals.

Neither Matsumura nor Yamada, either alone or in combination, disclose or suggest each of the features recited in claim 5. For example, neither of these references discloses or suggests the N buffers recited in claim 5, where each of the N buffers further include a high-priority queue for storing input packets having

a high priority and a low-priority queue for storing input packets having a low priority.

In rejecting claim 5, the Examiner points to Figs. 1 and 2 of Matsumura as disclosing the N buffers and the high priority queue and low priority queue recited in claim 5. (Office Action, pages 5 and 6). As discussed above with regard to the rejection of claim 1, Matsumura does not disclose or suggest N buffers that each include queues, and thus, Matsumura certainly could not disclose or suggest N buffers that each include the high-priority queue and the low-priority queue recited in claim 1. Figs. 1 and 2 of Matsumura disclose a temporary cell storage unit 20 or 30 that appears to include a number of queues or buffers. These queues or buffers, however, cannot be said to correspond to both the N buffers recited in claim 5 and the high-priority queue and the low-priority queue also recited in claim 5.

For at least these reasons, Applicant submits that, contrary to the Examiner's contentions, Matsumura does not disclose or suggest, as recited in claim 5, N buffers, each further including a high-priority queue for storing input packets having a high priority and a low-priority queue for storing input packets having a low priority. Applicant submits that Yamada also does not disclose or suggest these features of claim 5. Accordingly, Matsumura and Yamada, even if combined as the Examiner suggests, do not disclose or suggest each of the features recited in claim 5. The rejection of claim 5 is therefore improper and should be withdrawn. The rejections of claims 6-9 based are also improper and should be withdrawn, at least by virtue of the dependency of these claims from claim 5.

Independent claim 15 and dependent claims 16-18 were rejected under 35 U.S.C. § 103(a) based on Yamada in view of Matsumura.

Claim 15 is directed to a switching system that includes a plurality of input selector switches each configured to be connected to an input line and each receiving a system switching signal. The switching system of claim 15 further includes a first switch section and a second switch section connected to the plurality of input selector switches, one of the first switch section or the second switch section receiving packets from the plurality of input selector switches in response to the system switching signal indicating that either the first switch section or the second switch section is active, the first and second switch sections each including a buffer corresponding to each of the input selector switches, each of the buffers further including a plurality of priority queues for storing different priority packets from corresponding ones of the input selector switches. Further, the switching system includes a plurality of output selectors each connected to one of the buffers from the first and second switch sections; and a controller configured to generate the system switching signal and to receive status signals from the first switch section and the second switch section that include information relating to a state of the first switch section and the second switch section and being used by the controller to control the plurality of output selectors.

Neither Matsumura nor Yamada, either alone or in combination, discloses or suggests each of the features recited in claim 15. For example, neither of these references discloses or suggests a first switch section and a second switch section, the first and second switch sections each including a buffer

corresponding to each of the input selector switches, each of the buffers further including a plurality of priority queues for storing different priority packets from corresponding ones of the input selector switches.

In rejecting claim 15, the Examiner contends that Yamada discloses the recited buffer corresponding to each of the input selector switches, but concedes that Yamada does not disclose that each of the buffers further include a plurality of priority queues for storing different priority packets from corresponding ones of the input selector switches. (Office Action, pages 11 and 12). The Examiner relies on Matsumura for this feature. (Office Action, page 12).

Yamada is directed to a cell switching device capable of switching ATM cells between a first cell switch and a second cell switch. (Yamada, Abstract). Yamada discloses a cell switch 20 or 22 that each include a number of selector circuits 90, 92, 94, 96, 98, and 100. (Yamada, Fig. 1A). These selector circuits are disclosed by Yamada as including a single queue buffer that "temporarily stores the input cell under the control of the control circuit 134 while sequentially delivering such cells to the output port 48." (Yamada, Fig. 5 and col. 6, line 65 through col. 7, line 2).

Yamada appears similar to Matsumura in that both Yamada and Matsumura disclose a plurality of queues or buffers that store incoming cells in an ATM switchover system. Yamada, however, in no way discloses or suggests that a single queue, such as queue 132, can include a plurality of priority queues for storing different priority packets, as is recited for each of the buffers of claim 15. Likewise, Matsumura in no way discloses or suggests that the queues or buffers within temporary cell storage memory 202 (Fig. 3 of Matsumura) each

further include a plurality of priority queues for storing different priority packets. The queue 132 of Yamada and the queues or buffers within temporary cell storage memory 202 of Matsumura appear to be comparable structures within the devices of Yamada and Matsumura. Therefore, one of ordinary skill in the art would not be motivated to combine Yamada and Matsumura to include multiple queues from Matsumura within each of the queues of Yamada. Applicant submits that, if anything, Yamada and Matsumura teach away from the combination suggested by the Examiner. One of ordinary skill in the art, upon reading these references, would likely use either the queues of Yamada or the queues of Matsumura. Applicant submits, however, that there is simply no motivation to combine these references in the manner put forth by the Examiner.

As motivation for combining Yamada and Matsumura as suggested by the Examiner, the Examiner contends that "one is motivated as such in order to provide quality of service for higher delay priority cells over lower delay priority cells." (Office Action, page 12). Applicant submit that the Examiner's motivation is merely a conclusory statement regarding an alleged benefit of the combination. Such motivation is insufficient for establishing a *prima facie* case of obviousness.

For at least these reasons, Applicant submits that the rejection of claim 15 is improper and should be withdrawn. The rejections of claims 16-18, at least by virtue of their dependency on claim 15, are also improper and should be withdrawn.

Applicant respectfully requests that this Response under 37 C.F.R. § 1.116 be considered by the Examiner, placing claims 1-9 and 15-18 in condition for allowance. Applicant respectfully points out that the final action by

the Examiner presented some new arguments as to the application of the art against Applicant's invention.

In view of the foregoing amendments and remarks, Applicant respectfully requests the Examiner's reconsideration of this application, and the timely allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 CFR 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY SNYDER, L.L.P.

By: /Brian E. Ledell/
Brian E. Ledell
Reg. No. 42,784

11350 Random Hills Road
Suite 600
Fairfax, Virginia 22030
(571) 432-0800

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